UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,581	06/24/2003	Lyle E. Adams	63479.0109	1633

23309 7590 07/07/2005

Matthew J. Booth & Associates, PLLC
P O BOX 50010
AUSTIN, TX 78763-0010

EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 07/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,581	ADAMS ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *41-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *41-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the Applicant regards as his invention.

2. Claims 44, 45, and 46 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

3. Claims which combine description of a system on a chip semiconductor device with description of method for manufacturing it and description of method for using it, such as in Claims 44, 45, and 46, violate the second paragraph of 35 USC 112, since the purpose of that paragraph is to require the patentee to provide others with notice of boundaries of protection provided by patent, since a manufacturer or seller, at time of making or selling the structure set forth in the claims, would have no indication whether it might later be sued for contributory infringement if the structure is used in accordance with claimed method, and since the claims are thus not sufficiently precise that possibility of infringement may be determined with reasonable degree of certainty. *Ex parte Lyell*, 17 USPQ2d 1548 (BPAI 1990).

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 44, 45, and 46 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 44, 45, and 46 are multiply dependant upon Claims 41, which is a machine, and Claims 42 and 43, which are a process. Claims that are intended to embrace multiple statutory classes of invention (in the aforementioned claims, both a product or machine and a process), are precluded by the language of 35 U.S.C. 101 which sets forth statutory classes in the alternative only, and is also invalid under 35 USC 112, second paragraph, since claims which purport to be both machine and process are ambiguous and therefore do not particularly point out and distinctly claim the subject matter of invention. *Ex parte Lyell*, 17 USPQ2d 1548 (BPAI 1990).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the Applicant for a patent.

7. Claims 41, 42, and 43 rejected under 35 U.S.C. 102(a) as being anticipated by Palmchip Product Brief PALM-DP-2000 "AcurX Configurable SoC Platform" ("DP-2000").

8. In reference to Claim 41, DP-2000 teaches a system-on-chip (SOC) semiconductor device designed with a latency tolerant signal protocol, comprising: one or more processor cores (See 'Configuration Options Figure of Page 2, 'CPU'), one or more peripherals (See 'Configuration Options Figure of Page 2, 'Group D Peripherals' and 'Group E Peripherals'), one or more DMA-type peripherals (See 'Configuration Options Figure of Page 2, 'DMA Controller' and 'Group C Peripherals'), and a memory subsystem (See 'Configuration Options Figure of Page 2, 'Group B: Memory Subsystem'); a first internal bus coupled to said processor cores and to said peripherals (See 'Configuration Options Figure of Page 2, 'PalmBus'), said first internal bus uses an architecture with a latency tolerant signal protocol carries signals from signal initiators to signal targets; wherein said architecture with said latency tolerant signal protocol of said first internal bus provides for an arbitrary number of pipeline stages between any signal initiator and any signal target wherein said arbitrary number of pipeline stages are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration (See Page 3 Section 'Timing Tap Technology'); and a second internal bus coupled to said processor cores, said memory subsystem, and said DMA-type peripherals (See 'Configuration Options Figure of Page 2, 'MBus'), said second internal bus uses said architecture with said latency tolerant

signal protocol that carries signals from signal initiators to signal targets; wherein said architecture with said latency tolerant signal protocol of said second internal bus provides for said arbitrary number of pipeline stages between any signal initiator and any signal target wherein said arbitrary number of pipeline stages are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration (See Page 3 Section 'Timing Tap Technology').

9. In reference to Claim 42, DP-2000 teaches a method to manufacture a System-on-chip (SOC) semiconductor device designed with an architecture with a latency tolerant signal protocol, comprising: providing one or more processor cores (See 'Configuration Options Figure of Page 2, 'CPU'), one or more peripherals (See 'Configuration Options Figure of Page 2, 'Group D Peripherals' and 'Group E Peripherals'), one or more DMA-type peripherals (See 'Configuration Options Figure of Page 2, 'DMA Controller' and 'Group C Peripherals'), and a memory subsystem (See 'Configuration Options Figure of Page 2, 'Group B: Memory Subsystem'); providing a first internal bus coupled to said processor cores and to said peripherals said first internal bus uses an architecture with a latency tolerant signal protocol that carries signals from signal initiators to signal targets (See 'Configuration Options Figure of Page 2, 'PalmBus'); wherein said architecture with said latency tolerant signal protocol of said first internal bus provides for an arbitrary number of pipeline stages between any signal initiator and any signal target wherein said arbitrary number of pipeline stages are added during the floorplanning of the semiconductor device without requiring a

subsequent design or floorplanning iteration (See Page 3 Section 'Timing Tap Technology'); and providing a second internal bus coupled to said processor cores, said memory subsystem, and said DMA-type peripherals (See 'Configuration Options Figure of Page 2, 'MBus'), said second internal bus uses said architecture with said latency tolerant signal protocol that carries signals from signal initiators to signal targets; wherein said architecture with said latency tolerant signal protocol of said second internal bus provides for said arbitrary number of pipeline stages between any signal initiator and any signal target wherein said arbitrary number of pipeline stages are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration (See Page 3 Section 'Timing Tap Technology').

10. In reference to Claim 43, DP-2000 teaches a method to use a System-on-chip (SOC) semiconductor device designed with an architecture with a latency tolerant signal protocol, comprising: providing one or more processor cores (See 'Configuration Options Figure of Page 2, 'CPU'), one or more peripherals (See 'Configuration Options Figure of Page 2, 'Group D Peripherals' and 'Group E Peripherals'), one or more DMA-type peripherals (See 'Configuration Options Figure of Page 2, 'DMA Controller' and 'Group C Peripherals'), and a memory subsystem (See 'Configuration Options Figure of Page 2, 'Group B: Memory Subsystem'); carrying signals from signal initiators to signal targets with a first internal bus coupled to said processor cores and said peripherals, said first internal bus uses an architecture with a latency tolerant signal protocol (See

'Configuration Options Figure of Page 2, 'PalmBus'); wherein said architecture with said latency tolerant signal protocol of said first internal bus provides for an arbitrary number of pipeline stages between any signal initiator and any signal target wherein said arbitrary number of pipeline stages are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration (See Page 3 Section 'Timing Tap Technology'); carrying signals from signal initiators to signal targets with a second internal bus coupled to said processor cores, said memory subsystem, and said DMA-type peripherals, said second internal bus uses an architecture with a latency tolerant signal protocol (See 'Configuration Options Figure of Page 2, 'MBus'), said second internal bus uses said architecture with said latency tolerant signal protocol that carries signals from signal initiators to signal targets; wherein said architecture with said latency tolerant signal protocol of said second internal bus provides for said arbitrary number of pipeline stages between any signal initiator and any signal target wherein said arbitrary number of pipeline stages are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration (See Page 3 Section 'Timing Tap Technology').

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 41, 42, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 6,513,089 to Hofmann et al. ("Hofmann"), Applicant's Admitted Prior Art ("AAPA"), and US Patent Number 6,209,118 to LaBerge ("LaBerge").

13. In reference to Claim 41, Hofmann teaches a system-on-chip (SOC) semiconductor device, comprising one or more processor cores (See Figure 1 'PPC405 CPU'), one or more peripherals (See Figure 1 'I^2C', 'GPIO', and 'UART'), one or more DMA-type peripherals (See Figure 1 'DMA Controller'), and a memory subsystem (See Figure 1 'SDRAM Controller'); a first internal bus coupled to said processor cores and to said peripherals (See Figure 1 Number 101), said first internal bus carrying signals from signal initiators to signal targets (See Figure 1); and a second internal bus coupled to said processor cores, said memory subsystem, and said DMA-type peripherals (See Figure 1 Number 102), said second internal bus uses an architecture that carries signals from signal initiators to signal targets (See Figure 1). Hofmann does not teach

that said first internal bus uses an architecture with a latency tolerant signal protocol carries signals from signal initiators to signal targets; wherein said architecture with said latency tolerant signal protocol of said first internal bus provides for an arbitrary number of pipeline stages between any signal initiator and any signal target wherein said arbitrary number of pipeline stages are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration; said second internal bus uses said architecture with said latency tolerant signal protocol that carries signals from signal initiators to signal targets; wherein said architecture with said latency tolerant signal protocol of said second internal bus provides for said arbitrary number of pipeline stages between any signal initiator and any signal target wherein said arbitrary number of pipeline stages are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration. AAPA teaches that it is known in the art to construct the buses of an SOC device using pipeline stages, which provide a latency tolerant signal protocol. AAPA requires no set amount of pipeline stages, and thus, the number of pipeline stages used is arbitrary (See Page 4 Paragraph 8, Page 5 Paragraph 10, and Page 6 Paragraph 12). LaBerge teaches a system controller ASIC, which is equivalent to an SOC (See Figure 1 Number 30) containing programmable circuits, such as the pipeline stages of AAPA (See Figure 1 Number 80 and Column 3 Lines 44-55), that are designed into the chip from the beginning, but are not initially connected to the connection circuitry (See Column 3 Lines 22-33). The programmable circuits of LaBerge can then be selectively

connected to the connection circuitry without requiring a fundamental redesign of the chip (See Column 3 Lines 24-28 and 30-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hofmann with the use of pipeline segments on a bus of AAPA and the pipeline circuits laid out during floorplanning and capable of being connected to the interconnect bus at a later time, as taught by LaBerge, resulting in the invention of Claim 41, in order to enable shorter clock cycles by reducing the distance that must be traversed by a signal within a single clock cycle (See Page 4 Lines 15-23 of AAPA), to achieve higher operating frequencies and better performance (See Page 4 Lines 13-14 of AAPA), and to allow easier modifications of the circuit designs by designing the programmable circuits into the chip from the beginning so that they are available to implement modifications without a fundamental redesign of the chip (See Column 3 Lines 30-35 of LaBerge).

14. In reference to Claim 42, Hofmann teaches method to manufacture a System-on-chip (SOC) semiconductor device, comprising: providing one or more processor cores (See Figure 1 'PPC405 CPU'), one or more peripherals (See Figure 1 'I^2C', 'GPIO', and 'UART'), one or more DMA-type peripherals (See Figure 1 'DMA Controller'), and a memory subsystem (See Figure 1 'SDRAM Controller'); providing a first internal bus coupled to said processor cores and to said peripherals (See Figure 1 Number 101), said first internal bus uses an architecture that carries signals from signal initiators to signal targets (See Figure 1); and providing a second internal bus coupled to said

processor cores, said memory subsystem, and said DMA-type peripherals (See Figure 1 Number 102), said second internal bus uses an architecture that carries signals from signal initiators to signal targets (See Figure 1). Hofmann does not teach that said first internal bus uses an architecture with a latency tolerant signal protocol that carries signals from signal initiators to signal targets; wherein said architecture with said latency tolerant signal protocol of said first internal bus provides for an arbitrary number of pipeline stages between any signal initiator and any signal target wherein said arbitrary number of pipeline stages are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration; said second internal bus uses said architecture with said latency tolerant signal protocol that carries signals from signal initiators to signal targets; wherein said architecture with said latency tolerant signal protocol of said second internal bus provides for said arbitrary number of pipeline stages between any signal initiator and any signal target wherein said arbitrary number of pipeline stages are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration. AAPA teaches that it is known in the art to construct the buses of an SOC device using pipeline stages, which provide a latency tolerant signal protocol. AAPA requires no set amount of pipeline stages, and thus, the number of pipeline stages used is arbitrary (See Page 4 Paragraph 8, Page 5 Paragraph 10, and Page 6 Paragraph 12). LaBerge teaches a system controller ASIC, which is equivalent to an SOC (See Figure 1 Number 30) containing programmable circuits, such as the pipeline stages of AAPA (See Figure 1 Number 80 and Column 3 Lines 44-55), that are designed into the chip from the

beginning, but are not initially connected to the connection circuitry (See Column 3 Lines 22-33). The programmable circuits of LaBerge can then be selectively connected to the connection circuitry without requiring a fundamental redesign of the chip (See Column 3 Lines 24-28 and 30-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hofmann with the use of pipeline segments on a bus of AAPA and the pipeline circuits laid out during floorplanning and capable of being connected to the interconnect bus at a later time, as taught by LaBerge, resulting in the invention of Claim 42, in order to enable shorter clock cycles by reducing the distance that must be traversed by a signal within a single clock cycle (See Page 4 Lines 15-23 of AAPA), to achieve higher operating frequencies and better performance (See Page 4 Lines 13-14 of AAPA), and to allow easier modifications of the circuit designs by designing the programmable circuits into the chip from the beginning so that they are available to implement modifications without a fundamental redesign of the chip (See Column 3 Lines 30-35 of LaBerge).

15. In reference to Claim 43, Hofmann teaches method to use a System-on-chip (SOC) semiconductor device, comprising: providing one or more processor cores (See Figure 1 'PPC405 CPU'), one or more peripherals (See Figure 1 'I^2C', 'GPIO', and 'UART'), one or more DMA-type peripherals (See Figure 1 'DMA Controller'), and a memory subsystem (See Figure 1 'SDRAM Controller'); carrying signals from signal initiators to signal targets with a first internal bus coupled to said processor cores and to

said peripherals (See Figure 1 Number 101); carrying signals from signal initiators to signal targets with a second internal bus coupled to said processor cores, said memory subsystem, and said DMA-type peripherals (See Figure 1 Number 102). Hofmann does not teach that said first internal bus uses an architecture with a latency tolerant signal protocol; wherein said architecture with said latency tolerant signal protocol of said first internal bus provides for an arbitrary number of pipeline stages between any signal initiator and any signal target wherein said arbitrary number of pipeline stages are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration; said second internal bus uses said architecture with said latency tolerant signal protocol; wherein said architecture with said latency tolerant signal protocol of said second internal bus provides for said arbitrary number of pipeline stages between any signal initiator and any signal target wherein said arbitrary number of pipeline stages are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration. AAPA teaches that it is known in the art to construct the buses of an SOC device using pipeline stages, which provide a latency tolerant signal protocol. AAPA requires no set amount of pipeline stages, and thus, the number of pipeline stages used is arbitrary (See Page 4 Paragraph 8, Page 5 Paragraph 10, and Page 6 Paragraph 12). LaBerge teaches a system controller ASIC, which is equivalent to an SOC (See Figure 1 Number 30) containing programmable circuits, such as the pipeline stages of AAPA (See Figure 1 Number 80 and Column 3 Lines 44-55), that are designed into the chip from the beginning, but are not initially connected to the connection circuitry (See

Column 3 Lines 22-33). The programmable circuits of LaBerge can then be selectively connected to the connection circuitry without requiring a fundamental redesign of the chip (See Column 3 Lines 24-28 and 30-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hofmann with the use of pipeline segments on a bus of AAPA and the pipeline circuits laid out during floorplanning and capable of being connected to the interconnect bus at a later time, as taught by LaBerge, resulting in the invention of Claim 43, in order to enable shorter clock cycles by reducing the distance that must be traversed by a signal within a single clock cycle (See Page 4 Lines 15-23 of AAPA), to achieve higher operating frequencies and better performance (See Page 4 Lines 13-14 of AAPA), and to allow easier modifications of the circuit designs by designing the programmable circuits into the chip from the beginning so that they are available to implement modifications without a fundamental redesign of the chip (See Column 3 Lines 30-35 of LaBerge).

16. In reference to Claim 45, Hofmann, AAPA, and LaBerge teach the limitations as applied to Claims 41, 42, and 43 above. AAPA further teaches that a common solution in creating a pipeline is to insert a flip-flop in the path to capture and re-launch the signal (See Page 4 Lines 15-18).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hofmann with the use of pipeline segments on a bus of AAPA and the pipeline circuits laid out during floorplanning and

capable of being connected to the interconnect bus at a later time, as taught by LaBerge, resulting in the invention of Claim 45, in order to enable shorter clock cycles by reducing the distance that must be traversed by a signal within a single clock cycle (See Page 4 Lines 15-23 of AAPA), to achieve higher operating frequencies and better performance (See Page 4 Lines 13-14 of AAPA), and to allow easier modifications of the circuit designs by designing the programmable circuits into the chip from the beginning so that they are available to implement modifications without a fundamental redesign of the chip (See Column 3 Lines 30-35 of LaBerge).

17. In reference to Claim 46, Hofmann, AAPA, and LaBerge teach the limitations as applied to Claim 41, 42, and 43 above. Hofmann further teaches that the first internal bus and the second internal bus have an overlapping topology enabling both busses to access a plurality of common devices (See Figure 1), and that each topology is a bussed topology (See Figure 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hofmann with the use of pipeline segments on a bus of AAPA and the pipeline circuits laid out during floorplanning and capable of being connected to the interconnect bus at a later time, as taught by LaBerge, resulting in the invention of Claim 46, in order to enable shorter clock cycles by reducing the distance that must be traversed by a signal within a single clock cycle (See Page 4 Lines 15-23 of AAPA), to achieve higher operating frequencies and better performance (See Page 4 Lines 13-14 of AAPA), and to allow easier modifications of

the circuit designs by designing the programmable circuits into the chip from the beginning so that they are available to implement modifications without a fundamental redesign of the chip (See Column 3 Lines 30-35 of LaBerge).

18. Claims 41, 42, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hofmann, US Patent Number 6,594,814 to Jou et al. ("Jou") and LaBerge.

19. In reference to Claim 41, Hofmann teaches a system-on-chip (SOC) semiconductor device, comprising one or more processor cores (See Figure 1 'PPC405 CPU'), one or more peripherals (See Figure 1 'I^2C', 'GPIO', and 'UART'), one or more DMA-type peripherals (See Figure 1 'DMA Controller'), and a memory subsystem (See Figure 1 'SDRAM Controller'); a first internal bus coupled to said processor cores and to said peripherals (See Figure 1 Number 101), said first internal bus carrying signals from signal initiators to signal targets (See Figure 1); and a second internal bus coupled to said processor cores, said memory subsystem, and said DMA-type peripherals (See Figure 1 Number 102), said second internal bus uses an architecture that carries signals from signal initiators to signal targets (See Figure 1). Hofmann does not teach that said first internal bus uses an architecture with a latency tolerant signal protocol carries signals from signal initiators to signal targets; wherein said architecture with said latency tolerant signal protocol of said first internal bus provides for an arbitrary number of pipeline stages between any signal initiator and any signal target wherein said

arbitrary number of pipeline stages are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration; said second internal bus uses said architecture with said latency tolerant signal protocol that carries signals from signal initiators to signal targets; wherein said architecture with said latency tolerant signal protocol of said second internal bus provides for said arbitrary number of pipeline stages between any signal initiator and any signal target wherein said arbitrary number of pipeline stages are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration. Jou teaches that the use of pipelining is well-known in integrated circuit design (See Abstract), and the use of pipelines having a dynamically variable number of stages (See Column 1 Lines 55-58 and Column 2 Lines 12-17). LaBerge teaches a system controller ASIC, which is equivalent to an SOC (See Figure 1 Number 30) containing programmable circuits, such as the pipeline stages of AAPA (See Figure 1 Number 80 and Column 3 Lines 44-55), that are designed into the chip from the beginning, but are not initially connected to the connection circuitry (See Column 3 Lines 22-33). The programmable circuits of LaBerge can then be selectively connected to the connection circuitry without requiring a fundamental redesign of the chip (See Column 3 Lines 24-28 and 30-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hofmann with the use of pipelines having a dynamically variable number of stages of Jou and the pipeline circuits laid out during floorplanning and capable of being connected to the interconnect bus at a later time, as

taught by LaBerge, resulting in the invention of Claim 41, because pipelining is a well-known efficient technique for optimally designing high performance digital circuits (See Abstract of Jou), to achieve optimal pipeline speed (See Column 2 Lines 14-17), and to allow easier modifications of the circuit designs by designing the programmable circuits into the chip from the beginning so that they are available to implement modifications without a fundamental redesign of the chip (See Column 3 Lines 30-35 of LaBerge).

20. In reference to Claim 42, Hofmann teaches method to manufacture a System-on-chip (SOC) semiconductor device, comprising: providing one or more processor cores (See Figure 1 'PPC405 CPU'), one or more peripherals (See Figure 1 'I^2C', 'GPIO', and 'UART'), one or more DMA-type peripherals (See Figure 1 'DMA Controller'), and a memory subsystem (See Figure 1 'SDRAM Controller'); providing a first internal bus coupled to said processor cores and to said peripherals (See Figure 1 Number 101), said first internal bus uses an architecture that carries signals from signal initiators to signal targets (See Figure 1); and providing a second internal bus coupled to said processor cores, said memory subsystem, and said DMA-type peripherals (See Figure 1 Number 102), said second internal bus uses an architecture that carries signals from signal initiators to signal targets (See Figure 1). Hofmann does not teach that said first internal bus uses an architecture with a latency tolerant signal protocol that carries signals from signal initiators to signal targets; wherein said architecture with said latency tolerant signal protocol of said first internal bus provides for an arbitrary number of pipeline stages between any signal initiator and any signal target wherein said arbitrary

number of pipeline stages are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration; said second internal bus uses said architecture with said latency tolerant signal protocol that carries signals from signal initiators to signal targets; wherein said architecture with said latency tolerant signal protocol of said second internal bus provides for said arbitrary number of pipeline stages between any signal initiator and any signal target wherein said arbitrary number of pipeline stages are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration. Jou teaches that the use of pipelining is well-known in integrated circuit design (See Abstract), and the use of pipelines having a dynamically variable number of stages (See Column 1 Lines 55-58 and Column 2 Lines 12-17). LaBerge teaches a system controller ASIC, which is equivalent to an SOC (See Figure 1 Number 30) containing programmable circuits, such as the pipeline stages of AAPA (See Figure 1 Number 80 and Column 3 Lines 44-55), that are designed into the chip from the beginning, but are not initially connected to the connection circuitry (See Column 3 Lines 22-33). The programmable circuits of LaBerge can then be selectively connected to the connection circuitry without requiring a fundamental redesign of the chip (See Column 3 Lines 24-28 and 30-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hofmann with the use of pipelines having a dynamically variable number of stages of Jou and the pipeline circuits laid out during floorplanning and capable of being connected to the interconnect bus at a later time, as taught by LaBerge, resulting in the invention of Claim 42, because pipelining is a well-

known efficient technique for optimally designing high performance digital circuits (See Abstract of Jou), to achieve optimal pipeline speed (See Column 2 Lines 14-17), and to allow easier modifications of the circuit designs by designing the programmable circuits into the chip from the beginning so that they are available to implement modifications without a fundamental redesign of the chip (See Column 3 Lines 30-35 of LaBerge).

21. In reference to Claim 43, Hofmann teaches method to use a System-on-chip (SOC) semiconductor device, comprising: providing one or more processor cores (See Figure 1 'PPC405 CPU'), one or more peripherals (See Figure 1 'I^2C', 'GPIO', and 'UART'), one or more DMA-type peripherals (See Figure 1 'DMA Controller'), and a memory subsystem (See Figure 1 'SDRAM Controller'); carrying signals from signal initiators to signal targets with a first internal bus coupled to said processor cores and to said peripherals (See Figure 1 Number 101); carrying signals from signal initiators to signal targets with a second internal bus coupled to said processor cores, said memory subsystem, and said DMA-type peripherals (See Figure 1 Number 102). Hofmann does not teach that said first internal bus uses an architecture with a latency tolerant signal protocol; wherein said architecture with said latency tolerant signal protocol of said first internal bus provides for an arbitrary number of pipeline stages between any signal initiator and any signal target wherein said arbitrary number of pipeline stages are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration; said second internal bus uses said architecture with said latency tolerant signal protocol; wherein said architecture with

said latency tolerant signal protocol of said second internal bus provides for said arbitrary number of pipeline stages between any signal initiator and any signal target wherein said arbitrary number of pipeline stages are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration. Jou teaches that the use of pipelining is well-known in integrated circuit design (See Abstract), and the use of pipelines having a dynamically variable number of stages (See Column 1 Lines 55-58 and Column 2 Lines 12-17). LaBerge teaches a system controller ASIC, which is equivalent to an SOC (See Figure 1 Number 30) containing programmable circuits, such as the pipeline stages of AAPA (See Figure 1 Number 80 and Column 3 Lines 44-55), that are designed into the chip from the beginning, but are not initially connected to the connection circuitry (See Column 3 Lines 22-33). The programmable circuits of LaBerge can then be selectively connected to the connection circuitry without requiring a fundamental redesign of the chip (See Column 3 Lines 24-28 and 30-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hofmann with the use of pipelines having a dynamically variable number of stages of Jou and the pipeline circuits laid out during floorplanning and capable of being connected to the interconnect bus at a later time, as taught by LaBerge, resulting in the invention of Claim 43, because pipelining is a well-known efficient technique for optimally designing high performance digital circuits (See Abstract of Jou), to achieve optimal pipeline speed (See Column 2 Lines 14-17), and to allow easier modifications of the circuit designs by designing the programmable circuits

into the chip from the beginning so that they are available to implement modifications without a fundamental redesign of the chip (See Column 3 Lines 30-35 of LaBerge).

22. Claim 44 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hofmann, AAPA, and LaBerge as applied to Claims 41, 42, and 43 above, and further in view of US Patent Numbers 6,493,407 to Sheafor et al. ("Sheafor"), US Patent Number 6,173,349 to Qureshi et al. ("Qureshi"), and US Patent Number 5,469,547 to Pawlowski et al. ("Pawlowski").

23. In reference to Claim 44, Hofmann, AAPA, and LaBerge teach the limitations as applied to Claims 41, 42, and 43 above. Hofmann, AAPA, and LaBerge do not teach that signals are point-to-point and registered signals, and said latency tolerant signal protocol further comprises full handshaking. Sheafor teaches using registered signals on a bus (See Figures 2 and 3 and Column 5 Lines 24-53). Qureshi teaches the use of a point-to-point bus (See Column 1 Lines 16-30). Pawlowski teaches a signaling protocol that uses full handshaking (See Column 1 Lines 19-47).

It would have been obvious to one of ordinary skill in the ad at the time the invention was made to combine the device of Hofmann, AAPA, and LaBerge with the registered signals of Sheafor, the point-to-point bus of Qureshi, and the handshaking protocol of Pawlowski, resulting in the invention of Claim 44, because flip-flop interfaces are advantageous and serve to convert the unidirectional buses of the physical layer to a bi-directional bus arrangement (See Column 5 Lines 44-48 and Column 6 Lines 22-

24 of Sheafor); because point-to-point buses have lower latency, minimal bus contention, and the ability to support multiple simultaneous data transfers (See Column 1 Lines 26-28 of Qureshi); and because handshaking allows an asynchronous communication protocol to be used, which provide very high speed transfers of information between I/O devices and host computers and do not rely on a central clock which can limit the bandwidth (See Column 1 Lines 19-28 of Pawlowski).

Priority

24. Applicant's claim for domestic priority under 35 U.S.C. 119(e) is acknowledged. However, the provisional applications upon which priority is claimed fail to provide adequate support under 35 U.S.C. 112 for Claims 41-46 of this application. The claims contain subject matter which was not described in the specifications of the provisional applications in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Drawings

25. The drawings were received on 29 April 2005. These drawings are acceptable.

Response to Arguments

26. Applicant's arguments filed 29 April 2005 have been fully considered but they are not persuasive.

27. Applicant has argued the Examiner's determination that portions of the specification represent admitted prior art. In response, the Examiner notes that AAPA is being relied upon to teach that it is known in the art to construct the buses of an SOC device using pipeline stages, which provide a latency tolerant signal protocol. This is shown on Page 4 Lines 15-18, which states "The common solution to the problem of extended signal propagation times caused by the physical interconnect is pipelining - reducing the distance that must be traversed within a single clock cycle by inserting a flip-flop (also referred to herein as a register) in the path to capture and re-launch the signal." Further, as the Applicant has pointed out on Page 9 of the arguments, Paragraphs 9 and 12 describe the problems solved by the present invention, and thus disclose a previously known method of using pipeline stages in an SOC device.

28. In response to Applicant's argument that LaBerge is nonanalogous art, it has been held that a prior art reference must either be in the field of Applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the Applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this

case, LaBerge relates to methods for constructing ASIC's (or SOC's) in a more efficient manner by allowing extra unused elements (such as pipeline stages) to be incorporated into the design during layout and allowing the unused elements to be connected to the system on an as-needed basis, thus allowing changes without requiring a fundamental redesign of the layout.

29. In response to Applicant's argument that the use of Applicant's invention is different from the use of LaBerge, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963). As shown above, LaBerge in combination with Hofmann and AAPA, and, alternatively, LaBerge in combination with Hofmann and Jou teach each limitation of Claims 41, 42, and 43.

30. Applicant has argued that the Examiner has failed to consider all elements and limitations of Applicant's claims. However, the Applicant has not identified which elements and limitations the Examiner failed to consider.

Duty to Disclose

31. Applicant is reminded that each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in 37 CFR 1.56. Applicant is advised to submit any information material to patentability in accordance with 37 CFR 1.97 and 1.98.

Conclusion

32. The following prior art made of record and not relied upon is considered pertinent to Applicant's disclosure: US Patent Number 6,661,427 to MacInnis et al. and Palmchip Product Brief PALM-DP-1050 "PALMPAK Fast SoC Platform"; Palmchip CoreFrame View White Paper "Overview of the CoreFrame Architecture"; and IEEE 1999 Custom Integrated Circuits Conference Article "An Efficient Bus Architecture for System-On-Chip Design".

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The Examiner can normally be reached on Monday-Thursday (7-3:30), Alt. Fridays (7-2:30).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJC

Khanh Dang
Primary Examiner

Thomas J. Cleary
Patent Examiner
Art Unit 2111